ME 343 – Control Systems

Lecture 20

October 9, 2009

Root Locus – Phase lead compensator

$$D(s) = \frac{s+z}{s+p}, \quad p > z$$

Phase lead COMPENSATOR

Selecting z and p is a trial an error procedure. In general:

- The zero is placed in the neighborhood of the closed-loop natural frequency, as determined by rise-time or settling time requirements.
- The poles is placed at a distance 5 to 20 times the value of the zero location. The pole is fast enough to avoid modifying the dominant pole behavior.

The exact position of the pole p is a compromise between:

- Noise suppression (we want a small value for p)
- Compensation effectiveness (we want large value for p)

Root Locus – Phase lead compensator

Example: FPE 5.28

Root Locus – Phase lag compensator

$$D(s) = \frac{s+z}{s+p}, \quad p < z$$

Phase lag COMPENSATOR

Selecting z and p is a trial an error procedure. In general:

- The ratio zero/pole is chosen based on the error constant specification.
- We pick z and p small to avoid affecting the dominant dynamic of the system (to avoid modifying the part of the locus representing the dominant dynamics)
- Slow transient due to the small p is almost cancelled by an small z. The ratio zero/pole cannot be very big.

The exact position of z and p is a compromise between:

- Steady state error (we want a large value for z/p)
- The transient response (we want the pole p placed far from the origin)

Root Locus – Phase lag compensator

Example: FPE 5.27