

CHAPTER 7: APPLIED RESEARCH IN EUROPE

Though the Europeans have struggled for decades to be competitive in semiconductors, the fable of the tortoise and the hare comes to mind when contemplating the hazards in ignoring their relative strengths and strong ties in increasingly important applications areas. These tortoises have some harey friends.

1. Technology Mobilization Strategy

The European semiconductor industry is more strongly positioned in 1996, both technologically and financially, than at any time in well more than a decade. All the leading European semiconductor firms in 1996 are technologically far closer to the leading edge, qualifying fully integrated 0.35 micron (μm) CMOS manufacturing processes lines, and (the semiconductor divisions at least) have returned to profitability after years in the red.

This rebound has, in part, been facilitated through the coordination of the efforts of almost 200 European firms and research institutes through the 7 year (1989-96), \$3 billion cooperative program JESSI (Joint European Submicron Silicon), half funded by national governments and the European Union through the Eureka Program. Much of the semiconductor-related government funding in Europe has been channeled through JESSI. Plans are underway for a similar \$2.5 billion cooperative program, MEDEA (Micro-Electronics Development for European Applications) for 1997-2000. MEDEA will focus on technologies, designs, and methodologies for semiconductor applications in multimedia, communication and automobiles. On the order of 5-8 percent of both programs is/will be aimed at longer term applied research.

However, the European semiconductor suppliers have yet to see any real competitive improvement in terms of their share of world markets, which at less than 9 percent is only half of Europe's consumption share. Europe has competitive strengths in a few pockets, in particular in the small markets for EPROM and EEPROM memories, as well as in the much larger discrete components and analog devices (particularly mixed-signal ASICs) markets. Yet, the European semiconductor suppliers will likely be constrained in markedly increasing their market share for the foreseeable future, because of a number of factors. These include the relatively limited size of even the largest three (Philips, SGS-Thomson, Siemens), their weakness in the technology-driving and fast moving areas of DRAM memories and (especially) microprocessors and in design methodologies

and libraries, and the continued weakness of European equipment suppliers.

On the whole, the European semiconductor industry appears to spend more, as a fraction of sales (but considerably less absolutely), both on overall R&D and on applied silicon research than averages reported in the US by the Semiconductor Industry Association and the Semiconductor Research Corporation. This is because of the relatively limited scale of the European industry, relative to the ever increasing costs of keeping up with the technological forefront. The SRC estimates that the US spent \$274 million on the longer term applied research in semiconductors, less than 0.5 percent US merchant semiconductor sales estimated by the SIA of \$60 billion. This report estimates that European governments and industry are investing on the order of \$100-125 million annually (involving 700-900 researchers) in applied silicon research, or 0.7 to 0.9 percent of the \$13.5 billion size of the European industry in 1995.

However, the trend over the last 5 years in the major European semiconductor companies has been away from corporate funding of longer term research, toward nearer-term product-related development. Both Philips and Siemens, for example, went from corporate research labs that were 100 percent funded centrally, to where the product divisions were "contracting" for about 2/3 of the research activities in those corporate labs. The key European equipment maker ASMI in the Netherlands recently closed its applications lab. Further, in the UK the drop since 1990 in longer term industry research in semiconductors has been precipitous. Even the European Union R&D programs related to semiconductors are becoming more market driven. The result throughout Europe has been a large swing towards nearer term development.

In sum, the European strategy appears to be one that, particularly for cost and scale reasons, is content to remain (just) slightly behind the absolute worldwide technological frontiers—to let larger risk taking and forefront breakthroughs take place elsewhere—and, rather, to focus on niche applications markets where there are strong historic ties to world-competitive OEMs, and seek growth through embedding that systems expertise in mixed-signal and systems-on-a-chip applications, particularly in the telecommunications, multimedia, and automotive industries. Government funding and cooperative, coordinated R&D activities dominate in the applied silicon research area throughout the high tech Old Continent.

2. Locus and Funding of Applied Semiconductor Research

The main applied silicon research activities are undertaken through a number of reasonably well coordinated--and overlapping--activities. The two most important research groups in Europe for these longer term activities are at IMEC in Leuven, Belgium and the joint GRESSI organization in Grenoble, France, involving SGS-Thomson, France Telecom, and the French Atomic Energy Commission. European-wide coordination has occurred largely through JESSI and the European Union. Each is discussed below.

IMEC vzw today is the largest independent microelectronics research and development center in Europe.¹ By September 1996, IMEC employed nearly 650 people (if the more than 100 student researchers preparing masters and Ph.D. theses are included), about 85 percent of which are directly involved in R&D, mostly as scientists and engineers. The total budget in 1996 had to an estimated BEF 2.2 billion (about \$70 million).

IMEC collaborates closely on strategically important early stage research (deep submicron silicon and III-V processing, design methodologies, materials and packaging) and training with a large number of leading-edge companies and R&D organizations worldwide. Founded by the Flemish Government in Belgium in 1984, IMEC is an "Interuniversity Microelectronics Center" located in Leuven, Belgium. Thus, IMEC also has significant interaction and overlap (as described in more detail in Appendix 7-10) with the three Flemish Universities doing significant work in microelectronics (K.U. Leuven, Univ. Gent, and the Vrije Univ. Brussels). For example, the R&D activities of the INTEC laboratory of the University of Gent are fully coordinated with IMEC's activities.

IMEC's mission statement says that it performs "scientific research which runs 5 to 10 years ahead of industrial needs, with a view to practical applications." As such, a large fraction of the scientific and technical personnel, a rough estimate would be 200 (and \$20-25 million per year), are engaged in exactly areas of "applied silicon research." The other technical and scientific personnel are engaged in nearer-term development, in services such as prototyping for industry and universities, and in training. These services are described more fully in Appendix 7-10.

¹All information in the following description of IMEC is from public IMEC sources, including: "General Presentation of IMEC, 1996; "1995 Scientific Report," 1996, and "1995 Annual Report," 1996.

IMEC's overall R & D activities, described more fully along with IMEC's available infrastructure in Appendix 7-12, are concentrated on:

- the development of deep submicron processing technologies for future generations of ULSI chips;
- the development of novel design methodologies and tools for single chip systems and ATM;
- high-speed, high-frequency design & components for broadband and personal communication
- microsystems, sensors, solar cells, multi-chip modules, optoelectronic components, etc.;
- the support of the training of VLSI design engineers on behalf of both educational institutes and industry.

IMEC has grown rapidly in the last decade, despite—or perhaps because of—economic struggles, specifically of the European microelectronics industry, and more generally the deep European recession of the early 1990s. Its growth appears to reflect a trend among the major European semiconductor companies towards reducing their own in-house longer term research—along the 5-10 year horizon on which IMEC focuses—and focusing on the nearer term needs of their product divisions. IMEC's interaction with industrial partners, discussed in section 3, contributes a complementary source of expertise and funding as the costs for deep submicron research are increasing rapidly.

When considered on its own, the scale of "applied silicon research" at IMEC—the roughly 200 scientific and technical people—is impressive. IMEC applied silicon research alone appears to be comparable in scale to that of the applied silicon-related R&D undertaken in all of either France or Germany.

This is even more impressive considering the relative size of the research establishment in Belgium. IMEC scientific and technical staff in applied silicon is 1.1 percent of the country's entire research establishment.² Compare this to the less than 0.17 percent estimate of total national R&D spending that the SRC "Gap Analysis" suggested is accounted for by the \$274 million (and roughly 2700

² The OECD estimates that there were 18,105 full time researchers in ALL scientific and technical fields in Belgium. OECD in Figures: Statistics on the Member Countries, 1996 Edition, OECD, Paris, 1996.

researchers) invested in 1995 in similar longer term research by ALL actors in semiconductor research in the US.³

Besides IMEC, the second major locus of applied silicon research activities in Europe is GRESSI. Over the past decade, the French government has made a concerted effort to create a Silicon-Valley-like agglomeration of semiconductor expertise around Grenoble, and has located most government-controlled silicon research investments there. Since the French universities tend to concentrate on fundamental research, the result has been that the main bulk of the applied silicon research activities undertaken in France are done through the combined and closely coordinated activities in the Grenoble area of three parent organizations:

- SGS-Thomson Microelectronics (S-T);
- France Telecom's National Research Center for Telecommunications (CNET); and
- French Atomic Energy Commission's Laboratory of Electronics, Technology and Instrumentation (CEA-LETI).

The semiconductor-silicon-related (S-T/CNET/CEA-LETI) activities near Grenoble include about 500 scientists, engineers, and technicians (an estimated 150-200 of which do applied silicon research as defined in this report) across three cooperative foci, grouped roughly speaking as "back-end," "front-end" and "longer-term." While formally separate organizations, by most accounts these three groups operate in an integrated and coordinated way, with researchers from all three parent organizations working together (as well as those from Philips, which have joined and sent about 30 R&D personnel).

In 1990 CNET and CEA-LETI set up the GRESSI (Grenoble Submicron Silicon) cooperative effort. It coordinates most of the longer term work at CNET and CEA-LETI beyond the next generation (in 1996 largely 0.18 um and below).

GRESSI encompasses about 200 researchers from CNET and CEA-LETI, and makes up the bulk of the applied silicon research resources in France. According to the Director, funding is about \$50 million annually, and about half comes from the state-owned partners (France Telecom and the government's LETI research labs of the French Atomic Energy Commission) An additional 15-20 percent comes from the government through the EU and JESSI basic and long term

³ The OECD estimated that in 1995 the total R&D spending in the US was \$166 billion.

research program. The remaining 25-30 percent is from industry via royalties and licenses from S-T and other industrial partners, principally Philips and Matra-MHS.

GRESSI was originally set up under the auspices of the JESSI program with the aim of developing basic operations and modules of the CMOS, BiCMOS technological processes and EEPROM memories. Essentially, GRESSI does the longer term applied silicon research and then turns technologies over to the other two organizations. During 1995 it fabricated its first devices using 0.18 um processes, with plans to begin qualifying the 0.18 um process through the Centre Commun in 1998 for production by S-T and other partners like Philips starting in 1999/2000.

Together IMEC and GRESSI represent approximately half the applied silicon research resources in Europe. Both are significantly government subsidized: IMEC gets 45 percent of its budget from the Flemish government, and another 13 percent from the European Union. Because much of the rest of IMEC's budget comes from contract research for industry, often prototyping and other nearer term work, the Flemish government's importance in funding applied silicon is considerably higher. As noted, GRESSI receives only 25 to 30 percent of its funds from industry, with the rest coming from the French government and the EU.

Joint European Submicron Silicon project (JESSI)⁴

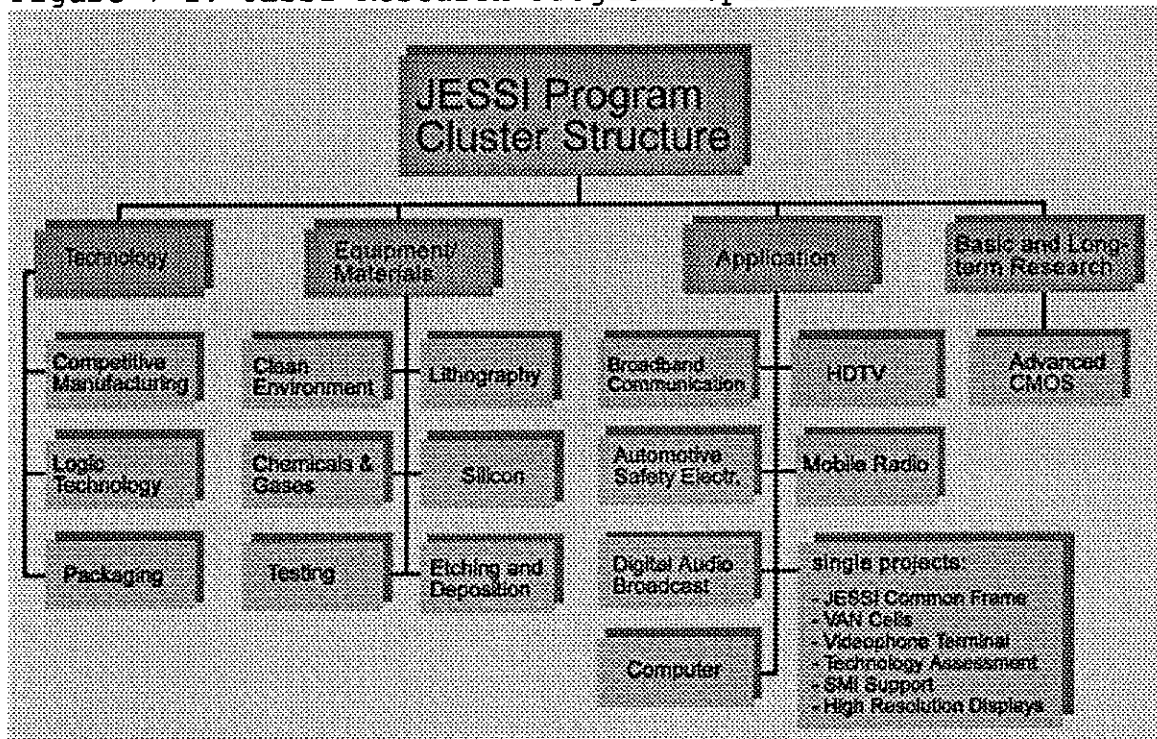
In addition to corporate and national efforts, there are several European cooperative R&D programs that also support applied silicon research: JESSI, JESSI follow-on MEDEA, and the European Union R&D programs like ESPRIT. To date the most important European-wide program has been the \$3 billion, seven year JESSI, which concluded at the end on 1996. Most government funding for semiconductor research outside the universities and public labs (or quasi-public groups like GRESSI or IMEC)--and even some of that when it is for cooperative projects--has been channeled through JESSI. That government funding was matched by industry. JESSI covered a wide swath in semiconductor-related micro-electronics, from broadband communications, to high-definition television, to process equipment, to longer term applied research in CAD tools, packaging, materials, and so forth.

⁴ Sources for data and program goals in this section are interviews with JESSI personnel, as well as: "What is JESSI," JESSI Office, Munich; the JESSI Office WWW homepage (www.jessi.org); the briefing book "JESSI: Joint European Submicron Silicon Program, EUREKA 127," JESSI Office, Munich (no date); and "JESSI In Brief: The Motivation for JESSI, a Cooperative R&D Programme on Microelectronics" JESSI Office, Munich (no date).

In a sentence, the program's supporters believed that the future strength of the European semiconductor industry depended on its ability to develop and competitively produce integrated systems-on-a-chip for key semiconductor applications markets, and JESSI helped fund and (more importantly) coordinate the development the whole package of competencies needed. A partial list of participating organizations is included in Appendix 7-3. Nearly 200 were involved--including most of the important European groups involved in applied silicon research--in more than 100 total projects. Financing from 1989-96 was provided 50% by the project partners, 38% by the many national public authorities and 12% by the Commission of the European Union.

According to the Director, about 6-8 percent of the research undertaken within JESSI was the longer-term applied research that is the subject of this study. The total JESSI resources in 1996 included about 2650 FTE researchers and about \$450 million. Thus, annual resources in applied silicon research coordinated through JESSI (and significantly overlapping with the resources reported elsewhere in this chapter) were about \$25-35 million, involving 150-200 researchers, or roughly $\frac{1}{4}$ of the estimated applied silicon activities in Europe. Expectations are that the JESSI-follow-on MEDEA program, discussed more below, will have a similar scale or resources and balance between short and longer term research.

Figure 7-1: JESSI Research Program Topics and Structure



Source: JESSI Office, Munich.

As shown in figure 7-1, JESSI was subdivided into four subprograms: Technology, Equipment/ Materials, Application and Basic & Longterm Research, which were further subdivided into 16 project clusters plus a number of "single" projects. The program and cluster structure of JESSI reflects the complexity of the program and the breadth of the industrial sectors involved. The structure of the JESSI program was based on its goal to strengthen the whole European electronics industry "chain": the electronic systems industry, the microelectronic components industry and the semiconductor production equipment and materials industry. The basic and long term research subprogram, which corresponded to the "Advanced CMOS" cluster where most of the applied silicon research of focus in this report fell, was intended to support and feed into all other parts of the JESSI program. All the projects for that subprogram were funded through EU programs.

(Very) Brief descriptions of the individual clusters and many of the JESSI Projects within these groupings are found in Appendices 7-1 and 7-2. Note there the emphasis on embedded systems applications, on related design technologies, and on integrating process modules for the next generation. In particular, the applications subprogram developed chipsets and design tools for systems

applications, particularly focusing on those areas where Europe has strong OEM systems suppliers, such as in telecommunications, multimedia and the auto industry.

Though many of the projects listed in Appendix 7-2 are not in the longer term applied research area, and have or are coming to a close, they are included there because they do demonstrate the strategic focus the Europeans have taken, and because the longer term aspects of JESSI were directed at supporting that focus. As the name of the planned follow on to JESSI indicates, the Micro-Electronics Development for European Applications program intends to focus even more closely on these systems applications areas.

Micro-Electronics Development for European Applications (MEDEA)⁵

MEDEA is a proposed pan-European R&D program, like JESSI, designed to enhance European competitiveness in microelectronics and related applications sectors. Unlike JESSI, it is not conceived so much as a process technology "catch-up" program. The thinking is that JESSI has helped Europe do that already. Rather, MEDEA will attempt to keep up with world frontier silicon technology platforms and manufacturing processes, improve (relatively weak) European deep submicron CAD design techniques, design tools and libraries, and have even greater focus than JESSI on applications areas. Like JESSI too, the initiative plans to bring together many of Europe's top electronics companies, both semiconductor and equipment and materials suppliers, as well as a host of user/applications firms.

MEDEA has been proposed for the Eureka Program by seven initial main sponsoring companies, all usual suspects, including semiconductor and equipment suppliers and users: Philips, Siemens, SGS-Thomson, Alcatel, Bull, Robert Bosch, and ASM International. Like JESSI, the program is open for participation by research organizations from any EUREKA participant nation. In June 1996 it was accepted in principle by government representatives at the Eureka Ministerial Conference and was announced. However, funding decisions will be made by the various national public authorities responsible for R&D funding. Hence, individual projects and participants within the broad parameters of MEDEA, as well as levels of funding, remain uncertain.

⁵ Information on MEDEA comes from the so-called MEDEA Yellow Book: "MEDEA: A Programme for the Micro-Electronics Development for European Applications, Eureka EU 1535, Yellow Book Programme Information-Update May 1996," JESSI Office, Munich, May, 1996, as well as from the MEDEA [www.homepage www.medeaa.org](http://www.homepage.www.medeaa.org).

Planned to cover four years 1997-2000, its estimated total cost will be about \$2½ billion, with approximately 1/5 of that during 1997. The plan calls for half this funding to come from public authorities and the other half from industry. The total four year program is expected to include about 12000 man-years of research effort. If the 6-8 percent estimate of the fraction associated with longer-term applied research holds true, then the annual manpower involved in applied silicon research in MEDEA will be approximately 200 FTE researchers, similar to JESSI. The distribution of resources from the various member countries is expected to be similar to that in JESSI, with perhaps less from the UK and more from the Netherlands: 29% France, 32% Germany, 19% The Netherlands, 10% Italy, 4% Belgium, 6% Rest of Europe. The annual distribution of researchers across various research areas is shown in table 7-1.

Table 7-1. Estimated MEDEA research resources, by area

Competence area	research man-years/year
Multimedia Technologies (chipssets, equipment-related)	700
Communications Technologies	600
Automobile & Traffic Applications	400
Design Techniques, Tools, Libraries	300
CMOS Based Technology Platforms	600
Manufacturing Technologies	400
Average Annual Total	3000

As technology and manufacturing benchmarks, the MEDEA roadmaps shown in Figures 7-2 to 7-4 are to enable Europe to by 2002 have commercial delivery from a fully integrated world-competitive 0.18 um (1.8V) CMOS manufacturing process generation (with 6 layers of metal) and the equipment, materials, and process technology for 300mm silicon wafers, and the corresponding design methodologies and CAD tools for systems-on-a-chip, with a focus on systems for multimedia, communications, and automotive/traffic applications. The commercial delivery of 0.25 CMOS systems on a chip with high density logic and memory (DRAM, FLASH, SRAM) is scheduled by 1999. The timeline also calls for 0.35 um high-density BiCMOS and embedded non-volatile memory (for smart card) capabilities by 1999, 0.18 um CMOS test chips of logic products from an industrial line by 2000, and 0.25 um very low-power (0.9V) capabilities by 2001/2.

[Figures 7-2, 7-3 and 7-4: MEDEA Roadmaps Here]

European Union R&D Programs⁶

The overall EU R&D budget over the period 1994-98 is 13.1 billion ECU (about \$16 billion), implemented through 18 thematic programs. The highest-funded single theme is "information technologies," via a \$2½ billion program called ESPRIT.

Esprit accounts for nearly all of the estimated \$25-30 million annual applied silicon research activities supported by the EU, roughly 0.8 percent of its overall R&D budget. Commission funding, then, represents roughly ¼ if the applied silicon research activities in Europe. Note that because the Commission funds projects at all of the main applied silicon research groups discussed in this chapter, there is considerable overlap with the funds reported here and those reported elsewhere—particularly the JESSI program: most of the longer-term research of JESSI was funded by the EU.

Begun in 1984, Esprit is targeted at R&D in a wide range of information technologies: for example, microelectronics, software, office systems, computer integrated manufacturing, and information processing. It is organized as a collection of independently managed projects under the "umbrella" strategic guidance of the Commission. The projects involve research on what the Commission calls "pre-competitive" technologies -- a catch-all phrase meaning technologies which are nearly-but-not-quite-marketable. About 40% of the organizations participating in Esprit projects are firms in "user" industries. Approximately 1/3 of participants are firms with fewer than 500 employees, 1/3 are large companies, and 1/3 are research institutes and universities.

⁶ Information on the European Union comes from: Esprit www homepage (www.cordis.lu/esprit/home.html), and from the following documents: "Information Technologies RTD Programme Domain 2: Technologies for Components and Subsystems, Summaries of Projects," Fourth Framework Programme, Directorate-General III--Industry, III/6383/96-EN, European Commission, Brussels, June 1996; "Information Technologies RTD Programme Domain 4: Long Term Research, Summaries of Esprit Projects, Working Groups and Networks of Excellence," Fourth Framework Programme, Directorate-General III--Industry, III/6383/96-EN, European Commission, Brussels, July 1996; "The Esprit Workprogramme, Edition 1996," Directorate-General III--Industry, European Commission, Brussels, 1996; "Advanced Research Initiative in Microelectronics (MEL ARI), European Commission, Brussels, December 1995; "Research and Technological Development Activities of the European Union, Annual Report 1995," COM(95) 443 final, European Commission, Brussels, 1995; "Research and Technology: the Fourth Framework Programme (1994-1998)" EUR 16620, European Commission, Luxembourg, 1995.

The 1996 ESPRIT work program is divided into eight broad research "Domains:"

1. Software Technologies
2. Technologies for Components and Subsystems
3. Multimedia Systems
4. Long-Term Research
5. The Open Microprocessor Systems Initiative
6. The High-Performance Computing and Networking
7. Technologies for Business Processes
8. Integration in Manufacturing

The most relevant domains for applied silicon research are 2 and 4. Domain 2, Technologies for Components and Subsystems (TCS), is funded at about 70 million ECU. It includes, *inter alia*, semiconductor components and subsystems, new materials, manufacturing and equipment, and efforts to improve competencies in advanced system-level design, in advanced analog and mixed signal design, and in testing. An estimated 2/3 of the component and subsystems work focuses on silicon, but activities also include compound semiconductors such as GaAs, InP, SiGe, particularly for high frequency or optoelectronic applications. Related work includes lithography, in-situ metrology and diagnostic tools. Interconnect and packaging related activities involve fine-line, multi-layer PCB manufacturing techniques and advanced device interconnection processes (including optical interconnect) and well as development of improved multi-chip module manufacturing technologies, and improved power/thermal performance packaging arrays.

Much of the TCS semiconductor-related work as of late 1996 was on the 0.18 μm CMOS generation, as the Commission had begun excluding 0.25 μm CMOS work from funding consideration. Of relevance to applied silicon research, there is also longer term work in advanced process technology modules for sub 0.18 μm CMOS technology.

Within Domain 4, Long Term Research, activities are grouped under an "Open Scheme" a "Reactive Scheme" and a "Pro-active Scheme." The first is open to research proposals at any time and of any information technology related "highly innovative" topic. It is intended to stimulate alternative approaches, novel and far-forward-thinking entrepreneurial ideas. In the reactive scheme, the projects respond to well identified industrial problems but are expected to be high risk. In the proactive scheme, the Commission has chosen two areas for focused long-term research programs, funded at about \$30 million each: "Intelligent Information Interfaces" (e.g. human interface)

and "Microelectronics Advanced Research Initiative (MEL-ARI)."

It is in this three year, \$30 million, MEL-ARI initiative where lie the relevant applied silicon activities outside of Domain 2. These activities are generally near the longer-run (10+ years out) tail of applied research, and might be considered fundamental. As of late 1996, these included two clusters of activities: one in optoelectronic interconnects (including light sources, detectors, chip design, architecture and packaging), and the other in nano-scale IC technology (devices, interconnects, fabrication processes and architecture). More details on these clusters of projects are in Appendix 7-6. Future clusters may be added.

However, the Commission generally sees its funding "window" to be fairly narrow: 4 to 7 years away from market applicability, i.e. not too short term or product oriented but not too long term or much beyond the second-to-next generation either. It sees its R&D role as complementary to the more fundamental work supported by most European governments and what it sees as industry's role in developing the next generation. As such, the Commission probably represents about 20-30 percent of the European research effort in the 0.18 um CMOS generation research "window," but it also does little beyond 0.13 um. Compare this to the Commission's 2 percent fraction of the overall European R&D pie across all industries.

The remaining applied silicon activities in Europe are thinly scattered throughout both industry and university/public sector laboratories. The most important other longer term industry research occur in the corporate labs and semiconductor divisions of Siemens and Philips, with more limited activities at Bosch and Daimler Benz's Temic group (in Germany), GEC-Plessey (UK), and Alcatel-Mietec in Belgium. Additionally, by world standards, the only major European presence in equipment occurs via ASM International and ASM Lithography (which is about 1/3 owned by Philips) of the Netherlands, who both do some related longer term research, often cooperatively with their suppliers.

The universities and government labs also play a role in applied silicon research, though the universities in Germany, France and the UK all tend toward more fundamental research. In Germany, the most relevant government labs are seven or eight of the 48 Fraunhofer Institutes, each of which is associated with a nearby university, and which are

funded by a combination of industry contract research, and contributions from the German Lander (states), federal government, and project-related European Union.

The Fraunhofer Gesellschaft (FRG) is the leading organization of applied research in Germany.⁷ Brief descriptions of the resources and activities of the Fraunhofer Institutes related to semiconductor research are given in Appendix 7-8. In general, the main research activities in the broad area microelectronics and microsystems can be summarized as follows:

- Technologies for high-level integration in silicon based circuits, including lithography, etching and deposition methods for CMOS, NMOS and bipolar technology, process simulation, and manufacturing equipment.
- III-V technology, e.g. GaAs for integrated circuits and optoelectronic components.
- Circuit design tools for the synthesis, analysis and verification of digital and analog circuits, diagnosis and testing of ICs, design automation.
- Development of digital, analog and mixed-signal circuits, standard circuits, semi-and full-custom ASIC, microwave circuits (MMIC), telecommunications
- Microstructure and microsystem technology, e.g. integrated sensors/actuators, packaging and interconnecting technology, prototyping.

The most important FRG institute for applied silicon research is probably the Institute for Silicon Technology (ISIT) in Itzehohe, because of its pilot Si-process line (150mm wafers, encompassing 3000 m² class 1 cleanroom). However, a significant amount of their pilot line capacity (one estimate was 80 percent) is contracted out to industry for prototyping, mostly by Daimler Benz's Temic semiconductor group.⁸ Given the mission of the FRGs to support local industry and the diffusion of existing technologies into German industry and the broader scope of

⁷ Information on the FRG from Die Fraunhofer-Gesellschaft von A bis Z: Institutsprofile, Forschungsgebiete, Leistungen, Ansprechpartner, Adressen, '96/97, Fraunhofer-Gesellschaft, Munich, 1996; and from "Profile of the Fraunhofer-Gesellschaft: Its Purpose, Capabilities and Prospects," Fraunhofer-Gesellschaft, Munich, 1995; and from "The Research Establishments: Addresses and Research Fields," Fraunhofer-Gesellschaft, Munich, May 1995. Also see the FRG homepage (www.fhg.de).

⁸ Temic is investing about \$50 million in expanding the FRG's Itzehohe facility to produce power ICs.

their activities than just in semiconductor silicon, a rough estimate for applied silicon research is 75-100 FTE researchers/students scattered throughout the FRG system and related university departments, encompassing spending on the order of \$12-15 million.

The majority of FRG activities is nearer term cooperative work with local small and medium sized businesses. Also partly relevant are the Max Planck Institutes, which are funded half by the federal government and half by the Lander, but their research is nearly exclusively fundamental (see Appendix 7-5).

In France, the main activities outside of Grenoble are in 25 or so of the 1500 research institute network of the government's national Center for Scientific Research (CNRS). CNRS works in close partnership with and often jointly operates the higher education sector's labs. Again much of the work is fundamental (see Appendix 7-11).

With the ending of the Alvey information technology program, the UK government has over the last 5 years or so largely gotten out of the business of funding industrially relevant applied semiconductor research. In part this is because British industry itself has had little interest: there remains relatively little indigenous longer-term industry research in Britain. The most important semiconductor-related enterprises in the UK are now foreign owned and/or have sharply curtailed their longer-range research. The emphasis has turned to more fundamental research in the universities, with limited pockets of applied activities, funded in large measure through the government's Engineering and Physical Sciences Research Council (EPSRC) and local Higher Education Funding Councils (see Appendix 7-9).

There are estimated to be fewer than 100 FTE researchers involved in applied silicon research in Britain, with less than \$15 million annually, and no real concentrated applied silicon research program anywhere. There are several universities with large groups of scientists doing semiconductor-related fundamental research, for example in quantum techniques, materials science, or solid state physics. Many if not all the UK university departments do have some collaborative research activities with industry. But, without the strong indigenous industry applied research programs to complement them, the net result--outside the possibility that fundamental research leads directly to novel and competitive approaches--is that it seems unlikely that Britain will play a significant role

in pushing the next several generations of semiconductor technologies.

3. Linking Applied Research to Business Outcomes

European semiconductor research strategies have increasingly focused on systems applications areas where they see themselves strategically better placed. Historically, the largest demand for semiconductors has come from computer markets, where US systems firms have had a dominant worldwide position, followed by consumer electronics, where Japanese systems suppliers had a clear edge. On the other hand, relative European systems strengths have been in other applications areas, such as telecommunications, industrial equipment, and automotive/transportation. Hence, applied research strategies increasingly are linked to business outcomes in these applications areas.

Each of the major semiconductor suppliers in Europe has strong current and historic ties to OEM companies competitive in one or more of these areas. They hope to exploit competencies in systems design and integration in the rapidly expanding markets in wireless and broadband communications, multimedia, and automotive applications. Given the Europeans' relative strength in analog and mixed-signal devices, if they can improve their design capabilities in these areas, then this strategy may payoff if those applications areas grow more rapidly over the next decade relative to DRAMs and microprocessors than they have in the past decade.

The most direct example of the links between applied research and business outcomes is the relationship between GRESSI and SGS-Thomson. As noted above, S-T is the single major beneficiary and industrial participant of GRESSI. In essence, GRESSI serves as S-T's "corporate" semiconductor R&D arm for longer-term activities, while the closely linked labs in the Grenoble area of CEA-LETI and CNET/S-T Centre Commun do nearer term work. The French government, in this way, heavily subsidizes S-T semiconductor research, through direct funding of CEA (and hence CEA-LETI), state ownership of France Telecom (and its CNET research arm) and via indirect subsidies through ownership of part of S-T and government contributions through JESSI, EUREKA and the EU.

Through co-location in Grenoble and close interaction among the research programs at CEA-LETI and the Centre Commun, the GRESSI applied research is integrated closely with S-T's technology and investment plans as well as those of France Telecom. Though S-T is smaller than the leading

semiconductor firms—its technology "roadmap" is consistent with worldwide frontiers, including production start on 0.18 um CMOS processes by 1999/2000. S-T capital investment and expansion plans are aggressive as well, with ongoing with upgrading of existing facilities and the recent announcement of the construction of two more 200mm (8") submicron fabs to be built in Italy and Singapore. These will join the two existing ones in Crolles (France) and Phoenix (Arizona), plus one fab now under construction in Rousset (France) and one nearing completion in Catania (Italy).

The Crolles fab near Grenoble also serves as the main testing and integration site for the processes and modules that come out of the R&D activities of GRESSI. The fully integrated 0.35 um processes now being used by S-T (and Philips) were transferred directly from the R&D undertaken at GRESSI and the Centre Commun. Plans are to similarly transfer and qualify 0.18 um (and below) modules and processes from GRESSI to the Centre Commun and to S-T over the next years.

By comparison to France, a far greater fraction of semiconductor research in Germany is funded by private firms, like Siemens. The most important applied silicon research activities in Germany are directly linked to business outcomes internally at Siemens, via their corporate research labs and Dresden Microelectronics Center.

Siemens has a broad product range across about 260 core business activities, mainly in high technology capital equipment and consumer goods. Product lines extend from electronic components and semiconductors, to communication networks and systems, computers, audio and video systems, automotive and transportation systems, to medical diagnostic systems, to industrial automation and power generation, transmission and distribution.

Note the importance of semiconductors in virtually all these applications areas, in many sectors of which Siemens is a market leader. For example, the Siemens-Nixdorf subsidiary is Europe's largest computer supplier, second only IBM in European sales. Similarly, Siemens is the premier European supplier for semiconductor chip sets for GSM cellular communications applications. One reason is that Siemens is Europe's largest OEM of GSM equipment. In multimedia, Siemens claims to have been first to market with a combined multimedia terminal, which integrates a PC, TV, phone and fax in one system. Siemens is also among the top 10 automotive electronics suppliers worldwide.

Since 1994, Siemens has moved from a policy where corporate research was 70 percent funded at the corporate level, to a system much more driven by the product divisions: only about 35 percent of the Siemens corporate research is now funded at the corporate level (which tend to be more open to longer term applied research). Now, 50 percent comes from contracts with divisions. The rest is public funds. The net result has been a trend over the last few years in the German facilities of Siemens away from applied silicon work, towards nearer term developmental activities, and explicit corporate pressure on the applied work that remains to more closely link to the business needs of Siemens' diverse product divisions.

Specifically as a semiconductor supplier, Siemens' semiconductor group was during the latter part of 1996 bringing into process ramp-up what is Europe's most advanced semiconductor manufacturing process line, for volume production of 64 MB DRAM chips. This is located at the new Siemens Microelectronics Center Dresden (SIMEC).⁹ However, much of Siemens' most intense CMOS process technology research activities are done cooperatively in conjunction with IBM and Toshiba at IBM's Fishkill research facilities in the US. The SIMEC facility also will have a research and pilot line using 0.25 um technologies developed in conjunction with IBM and Toshiba. Recently, Motorola agreed to join the IBM/Siemens/Toshiba trio for development of integrated 0.18 um process and device technologies needed for a 1 Gigabit DRAM chip. About 80 Siemens researchers are working on these joint activities on location at IBM's Fishkill facilities in the U.S.

In Germany, Siemens is followed by a scattering of applied silicon research activities throughout several Fraunhofer research institutes. The FRG mission is to support local industry and the diffusion of existing technologies into German industry. R&D can be commissioned by industrial companies, and tends to be directed towards local small and mid-sized firms needing technical assistance. As a result, the silicon related R&D work of the FRG institutes tends towards nearer term development work, such as in designing ASICs and fabricating prototypes.

These are followed by limited activities at Daimler Benz, related to applications by its Temic semiconductor group, and at Robert Bosch, related to its applications particularly in the automobile and industrial machinery

⁹ See Harald Eggers, "Das Siemens Microelectronics Center in Dresden," in Siemens Zeitschrift: Innovation durch Forschung und Entwicklung, Fruhjahr (Spring) 1996, pp. 27-31.

sectors. Despite Daimler Benz's position among the 30 largest firms in the world,¹⁰ Temic has no illusions about being a world leader in semiconductor technology. Its current and future roadmap for process technology implementation in its wafer fabrication facilities is at least a generation behind world-class targets. Indeed, its most advanced manufacturing facilities now are actually those it subcontracts from the Fraunhofer Institute for Silicon Technology (ISIT) in Itzehoe.

Temic's semiconductor activities are simply too small to support the huge expenses needed to be pushing the forefront. Temic has been content to license/acquire technologies and equipment developed elsewhere, and integrate them with their areas of applications expertise. Rather, its research activities are centered on what Temic sees as its core competencies, in RF design and technology, automotive IC design, controller architectures, low-voltage, low on-resistance MOSFET, and power IC technologies, and mixed-signal ASIC design and supply, and optoelectronics.¹¹ Moreover, at the Daimler Benz corporate level, corporate research has, like elsewhere in Europe, been asked to get the bulk of its funding from the product divisions. So again, like elsewhere in Europe the link between research and business outcomes lies in applications in automotive, telecommunications, and multimedia.

The applied research at IMEC in Belgium is similarly undertaken with a strategic eye on business outcomes, though IMEC is not directly linked to any for profit business. IMEC arose from a Flemish Government program in microelectronics set up in 1982. The program aimed to strengthen microelectronics industry in Flanders (particularly to solidify and strengthen the local activities of Alcatel). This decision was inspired on the one hand by the strategic importance of microelectronics for industry and on the other hand by the major investments required to keep up with the industry's technological frontiers. This program included the establishment of a laboratory for advanced research in microelectronics (IMEC), the establishment of a semiconductor company (MIETEC) which is now a 100% subsidiary company of Alcatel and the organization of a training program for VLSI design engineers which is now fully integrated in the IMEC activities.

As part of this goal to increase the strength of the Flemish semiconductor industry, IMEC fosters an intentionally high employee turnover rate, near 17 percent

¹⁰ Fortune Magazine, Global 500 list, 1996.

¹¹ Temic www homepage (www.temic.com).

per year. As one result, IMEC has been an incubator for at least eleven spin-off companies in Belgium, three within the first half of 1996.

However, business interest in access to IMEC facilities and expertise goes well beyond Flanders: IMEC appears to be rapidly attracting worldwide attention. In 1995, IMEC collaborated with 365 companies and research institutions from 37 countries. Most of the bilateral or multilateral contract research takes place through IMEC's "in-situ" Industrial Affiliation (IIAP) or Industrial Residency Programs, described in more detail in Appendix 7-10. Through these programs IMEC offers specially tailored R&D cooperation. Partners gain access at an early stage to strategic background information required for the completion of their projects. Partners pay for access to and use of IMEC background information, as well as for the completion of the project. With regard to intellectual property rights over the results, IMEC distinguishes between joint property rights over the results that are based on IMEC's background information and the exclusive property rights that the partner has in the more industrially oriented results. This approach has attracted small and large corporations worldwide, including Intel, Motorola, TI, Sony, AMD, National Semiconductor, LAM, Ashland Chemicals, ASML, Philips, Siemens, Alcatel, and many others.

IMEC's own technologies (including processing, components, detectors, software tools for chip design, device modeling, manufacturing science, reliability, characterization and analysis, testing) can be transferred to industry for further development and/or commercialization via license agreements. License agreements of this kind can be entered into either alone or in combination with the 'in-situ' programs.

At present the Industrial Affiliation-research domains are mainly oriented to those process technology steps and modules where IMEC has focused on developing leading-edge capabilities (sub 0.25 μm optical lithography; cleaning and ultra clean processing; advanced metallization; Environment, Safety and Health; and also nano-probe analysis). New research domains areas are in being launched such as sub 0.1 μm device physics.

Moving on to the linkage between applied research and business outcomes in the European-level programs, Siemens, S-T, and Philips are very active in the cooperative European programs. Indeed, they were among the 12 companies most responsible in the early 1980s for promoting the formation

of the European Commission's Esprit program, the granddaddy and still largest of the current EU R&D programs. They are also among the founding members of JESSI and most recently MEDEA. Industrial partners in these programs pay upward of half their costs. Unsurprisingly, the strategic foci of these European programs have increasingly turned to applications and embedded systems-on-a-chip areas very much in line with those in which European firms, S-T, Siemens and Philips in particular, are strong in world markets: telecommunications, automotive applications, and multimedia.

Both JESSI and MEDEA are industrially driven with respect to goals and procedures and governed by management boards led by industry representatives (see Appendices 7-3 and 7-4). JESSI was set up with the explicit mission to link research to the following business outcomes:

- Accelerate the progress of European integrated circuit suppliers;
- Enhance the competitiveness of European system houses;
- Expedite the market introduction of innovative system concepts;
- Stimulate the availability of advanced design methods and tools;
- Strengthen the position of European semiconductor equipment and materials suppliers;
- Intensify cooperative relations within the industry chain.

MEDEA will continue JESSI's focus on harnessing existing European strengths in telecommunications, multimedia, and automotive applications areas and on their worldwide market potential. The perceived importance of MEDEA for the Europeans lies in the growing role that semiconductors play in those industries. The proportion of electronic systems that can be integrated into silicon chips is rising rapidly, giving an increasing potential advantage to OEM's who can make early use of the most advanced semiconductor technologies. MEDEA forecasts that the semiconductor content in electronic systems will increase to 23% by 2000 from the 1996 average of 16%. In MEDEA's founders' view, this makes it strategically vital for Europe to have world class capability not only in the volume production of advanced semiconductor devices but also in integrating that with applications expertise. Because of this focus, MEDEA plans to deliver chipsets and other key components designed to give Europe's systems manufacturers in these applications areas a competitive edge.

The applications MEDEA will focus on are:

- chipsets for multimedia interactive user terminals and multimedia signal processors, high security and contactless chip (smart) cards;
- communication, in particular broadband networks and wireless communication and other key trends in communication towards digitization, mobility, data compression, standard network interfaces and new services (e.g. chipsets for advanced wireless multi-standard--GSM, DECT, etc.--multi-service terminals, low power open/modular digital signal processors, standardized broadband network interfaces);
- automobile control functions and in-car traffic systems (e.g. harsh environment technologies, adaptive learning control circuits, speech recognition with learning in noisy environment).

These applications areas are tied together in MEDEA with deep submicron design tools and technology mapping, systems on a chip and high level design techniques, and applications related methodologies and macro libraries, as well as with the 0.25 and 0.18 um and multifunctional CMOS technology platforms, and 300 mm manufacturing technologies and fab design.

Also included are selected new equipment and materials needed by the technology platforms. These include:

- advanced lithography equipment (deep-UV, step and scan, related technologies);
- cluster tools and furnaces (hot and lower temperature processing, batch and rapid thermal processing, in-situ metrology) together with gases and chemicals;
- clean room technology;
- silicon (300 mm, SOI, SiGe);
- metrology and testing.

The European Union Programs are also generally focused on business outcomes. Though not governed by industry in the way JESSI and MEDEA are, the European Commission nonetheless cooperates closely with industry in establishing research priorities. Specifically, the EU seeks its niche in filling gaps the Commission and its business advisory groups see between product oriented research private industry is supporting, and the fundamental science funded by the national governments.

Esprit has a so-called "rolling work-program," adapted each year, after consultation with industry, to take account of industry's changing priorities, and contains descriptions of the tasks to be undertaken. A Commission task force, drawn mostly from industry, works closely with industrial leaders to set out the strategic goals and targeted technologies. The Commission then invites proposals from consortia of interested parties for carrying out R&D projects in priority areas. Industry is free to work out its own cooperative R&D consortia in order to tender proposals. But, to be considered, projects must involve at least two independent firms from different EU member or "associated" nations. As Appendix 7-7 describes in a bit more detail, organizations from other countries are eligible to participate, and have access to the research results, but not receive EU funding. In the spirit of keeping research support linked to areas of significant interest to business, most Community-funded research projects are what are called "shared-cost actions," where Community participation in R&D costs is normally not more than half of the total project costs for industrial partners.

The various ESPRIT programs have, since 1984, aimed to develop enabling technologies, to foster European collaboration and to lay the foundations for European standards. More specifically, in 1996 the Esprit Program's main goals were explicitly business outcome oriented:

- to ensure that Europe's professional software developers continue to have the skills, capabilities and key technologies to provide competitive software intensive systems;
- to encourage better and more competitive technologies for the manufacture and use of electronic components and subsystems;
- to support strategic research and technological development in the generic information technologies for multimedia end-user systems and applications;
- to support long term research with a view to maintaining the potential for the next wave of innovation and to replenishing scarce expertise in key areas.

At the same time, Esprit proponents emphasize that, because European markets are fragmented by national borders, the communication channels required for technology sharing are inadequately developed. A related concern is that Europe

has been weakest in moving technologies from the laboratory to downstream applications in the marketplace. The policy response here is that Esprit explicitly stresses not only the development of new pre-competitive technologies, but also diffusion and vertical links along the technology food chain. A significant fraction of the Esprit budget is aimed at increasing the use of existing technologies by small and medium sized enterprises, on "marriage brokering" among firms, universities, and other research groups, and on generally improving communication within and among professional social networks. Indeed, Esprit is often characterized as a diffusion oriented R&D program.

Along those lines, the rules which the Commission imposes on Esprit participants stipulate that any technical information or patents resulting from work on an Esprit project must be made freely available to all partners in the project. The Commission also reserves the rights to publish reports on all Esprit work, and to require commercial licensing of results to other companies if a firm fails, without a legitimate reason, to exploit technologies it developed under Esprit.

As with JESSI and MEDEA, Esprit's application's emphasis is on communications, automotive and consumer electronics and industrial applications, traditional areas of competitive strength for European OEM's. Applications research is aimed at improved portability, endurance, power efficiency, power control, and at development of multifunctional systems. Domain 2 work also includes microsystems, flat panel displays, and advanced mass storage devices.

Given current European weaknesses in design and design libraries, Domain 5, the \$30 million Open Microprocessor Initiative, though generally nearer term than the applied silicon research of interest in this study, is also relevant in terms of Europe's strategic outlook and focus on business outcomes in particular applications areas. Launched in 1992, OMI brings together silicon manufacturers, systems tools companies and some smaller vendors, embedded software houses (compilers, operating systems, real time operating systems, ranges of kernels) and system integrators.¹²

OMI's objective is to promote innovation in the components of embedded microprocessor systems, including software, tools, and methodology. It has a major aim of improving the inter-operability and re-usability of the

¹² Details on OMI from its homepage (www.omimo.be) and the Esprit sources listed above.

components in order to improve productivity in the target area of embedded systems, specifically in applications areas telecommunications automotive and transport, consumer electronics and multimedia, smart cards, and industrial and process controls. In 1996, OMI consists of over 40 projects, involving over 400 companies, universities and research establishments. Much of the early work was geared to making the "system on a chip" more open and allowing the trading of intellectual property (e.g. in designs) between companies (various standards and guidelines were developed in this process) with real applications providing demonstrators to prove the concepts in practice. Now, targeted tasks include contributing new hardware "cells" to open-licensing design libraries, including microprocessors, microcontrollers, digital signal processors, and application specific cells. Participants add elements to a library of appropriate open systems software and tools. The resulting inter-working components cover a wide range of systems performance and functionality. Although OMI is primarily a European venture it also welcomes participation from non-European firms.

In sum, the goals, justifications, and strategy of linking R&D to business outcomes of the European Union programs are similar to those of JESSI and MEDEA under the Eureka Program. The target applications areas are similar. Each program emphasizes the importance of innovation, diffusion, and research cooperation in facing Europe's relative industrial decline, its chronic unemployment, and the technical dominance of American and Japanese firms in large segments of world markets. They are geared to avoid duplicative research efforts, enable adequate economies of scale and scope, promote diffusion and spread R&D risks. This is put succinctly in the *Eureka Declaration of Principles*, under which JESSI and MEDEA operate:

"The objective...is to raise, through closer cooperation among enterprises and research institutes in the field of advanced technologies, the productivity and competitiveness of Europe's industries and national economies on the world market, and hence strengthen the basis for lasting prosperity and employment...."¹³

In JESSI, MEDEA and EU programs alike, industrial, university, and other research institutes come together in cooperative R&D consortia which are partly funded by governments. In each program, an umbrella governmental organization attempts to facilitate bringing research partners together, under the assumption that partners had been unable or unwilling to come together before. In each,

¹³ Declaration of Principles Relating to Eureka (1985) p. 80.

the umbrella organization oversees a large number of independently funded and managed projects. Firms are free to select their own partners, and free to select technologies on which they wish to work. The international R&D consortia are seen as a solution to innovative failures, rigidities in the flows of technical information, and the resulting European competitive weakness in international markets.

Figure 7-2

Interdependencies between Applications, Processes and Equipment:

	MULTIMEDIA	COMMUNICATION	AUTOMOTIVE	CHIPCARDS
DESIGN TECHNOLOGY	• SPEED OPTIMISED	POWER OPTIMISED LIBRARY	MIXED SIGNAL	LIBRARY
	• AREA OPTIMISED LIBRARY			
		0.35µm LOW-POWER	0.5µm-0.35µ BICMOS/POWER	0.35µ NVM
PROCESS TECHNOLOGY	0.18* µm 0.25 µm 0.35 µm	BASE LINE	CMOS	
EQUIPMENT +MATERIAL	EQUIPMENTS } FOR }		0.25µm on 200 mm PILOT LINE for 300 mm	PRODUCTION

* 0.18 µm is partially available only

Figure 7-3

The MEDEA CMOS LOGIC ROADMAP foreseen:

	1997	1999	2002
Feature size (µm)	0.35	0.25	0.18
Gates/chip	2.5 M	5 M	10 M
Chip Size (mm ²)	> 200	400	600
Max. No. of Wiring levels	4-5	5-6	6
Power Supply Voltage (V)	3.3 - 2.5	3.3 - 1.8	2.5 - 1.5
Chip Frequency (MHz)	200	300	> 400
Embedded Memory size (SRAM)	512 K	1-2 M	4 M
No. of I/O	> 200	> 500	1000

Figure 7-4

MEDEA OPTIONS - TECHNICAL CAPABILITY Foreseen:

NVM (for smart card)	*		*		
	0.5 μm		0.35 μm		
LOW-POWER SUPPLY VOLTAGE	*		*		
		0.35 μm 1.8 V		0.25 μm 0.9 V	
BICMOS	*		*		
	0.5 μm (Hi-SPEED)		0.35 μm (Hi-DENSITY)	0.35 μm (Hi-SPEED)	
*CMOS BASIC LOGIC PROCESS	*		*		
	0.35 μm 3.3 V		0.25 μm 3.3 -1.8 V		0.18 μm 2.5-1.8 V
Year	1997	1998	1999	2000	2001/-2

Themes to be worked on with priority:

- Theme 5.1 0.25 micron CMOS Basic Logic Process:**
Commercial delivery of 0.25 micron CMOS in products by 1999 on a chip with high density logic and high density memory (DRAM, FLASH, SRAM)
- Theme 5.2 0.18 micron CMOS Basic Logic Process**
Silicon of testchip for 0.18 micron logic products available in an industrial line by 2000
- Theme 5.3 Multifunctional Processes:**
Addressing specific application, availability of 0.35 micron analogue will be by 1998, 0.35 micron BICMOS embedded non volatile memory by 1999 and 0.25 micron very low voltage around 2000