PUBLICATIONS


TECHNICAL MEMORANDA

1. A 3-Terminal Model for Diffused and Ion-Implanted Resistors
2. N-Section R-C Models for Integrated Resistors
3. The AUSSIM MOSFET Model
4. The RSIM MOSFET Model
5. S-Parameter Measurements and Modeling for 0.25mm MOSFET’s
6. The AMC Compact Model Compiler
7. The Effect of Feed-back Delay on the Noise Response of the Phase-Locked Loop
8. Analog and Simple Behavioral Verilog Models for the Dual-Loop Phase-Locked Loop
9. Clock Signal Jitter Metrics
10. PLL stability at low ratios of phase-detector frequency to PLL bandwidth
11. Crystal-oscillator simulation using a Q-controllable behavioral crystal model
1. A 50% duty-cycle preserving 1 to 8 divider cell which requires no reset
2. Voltage-controlled oscillator delay cell for phase-locked loop
5. Software and methodology for schematics-based full-chip place-and-route layout
7. Glitchless clock and levels MUX that is frequency independent and does not need inputs to be synchronous or have integer relationships
8. Unit-cell layout technique for current-mirror components
10. A global reference current distribution scheme with programmable bias controls and compensation for process, voltage and temperature variations.
11. Differential output buffer with switched internal load to maintain common-mode feedback steady-state during disable state
12. Programmable Divider with relative Phase Delay or Advance for PLLs with Multiple Outputs: United States Patent 7,586,344 September 8, 2009
13. Combined Variable Gain Amplifier and Analog Equalizer Circuit
14. Shared-Array Multiple-Output Digital to Analog Converter
15. Method of delaying data from clock in 1UI steps
16. Expandable shift-register for Decision-Feedback Equalizer
17. Phase-locked loop circuit with selectable feedback paths
18. Power control block with output glitch protection