A Five-input Majority Gate in Quantum-dot Cellular Automata

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ABSTRACT

Quantum cellular automata (QCA) is expected to provide highly dense nanotechnology implementations of logic. However, unlike the CMOS technology, the designs in QCA are constrained by the limited number of basic gate structures. This paper describes an important new basic building block, a five input majority gate (MAJ₅) in QCA technology. Many new functions can be directly implemented in a single MAJ₅ gate. We demonstrate its use in a bit-serial adder. Since the designs using this gate generally use a smaller number of gates, wires and wire crossings, these designs are less susceptible to faults such as missing cells. This paper also presents a modified MAJ₅ gate with a greater fault tolerance.

 ${\it Keywords}:$ nanoelectronics, QCA, five input majority gate

1 INTRODUCTION

Over the years, engineers have been able to continuously shrink the size of CMOS transistors and thereby package more of them on the same chip. However, as we approach the physical limits of photo-lithography as well as device physics, this task has become more expensive and complicated. Studies show that the progress towards increasing chip complexity while maintaining the speed and constraining the power dissipation has slowed considerably. It is now believed that within the next two decades, the semiconductor industry will have to start using new nanoelectronic devices [1]. The international roadmap for semiconductors has enumerated several nanoelectronics alternatives including Resonant Tunneling Diodes (RTD), Quantum-dot Cellular Automata (QCA), Tunneling Phase Logic (TPL), and Single Electron Tunneling (SET) [2]. Amongst all these technologies, QCA promises to provide the highest device density with the low power consumption and high switching speeds [3]. In addition, QCA uses the same technology to build both, the logic gates and the wires carrying logic signals.

Even though QCA has attractive properties, building large QCA architectures has not been very successful. The primary limitation to QCA is the availability of only two basic building blocks: an inverter and a three input majority gate (MAJ_3) shown in Fig. 1. Though the MAJ_3 gate can be configured as a two input AND or OR gates, building larger architectures with two input gates is laborious. Such architectures tend to have high complexity, difficult connectivity and low reliability.



Figure 1: The only gates in QCA technology: a three input majority gate MAJ_3 (left) and an inverter.

This paper introduces a new powerful building block for QCA technology, a five input majority gate (MAJ_5) . We show its generality in implementing other functions and demonstrate its applicability through a serial adder that uses only one MAJ_3 gate and an inverter besides the new MAJ_5 gate. We also provide a more robust version of the MAJ_5 gate which functions correctly in more than 40% of the cases of missing a single QCA cell in the structure.

2 QUANTUM CELLULAR AUTOMATA (QCA)

Quantum cellular automata (QCA), first proposed in 1993 by Tougaw and Lent [4], is a structure made up of identical cells realized though a variety of technologies such as electrodynamic, ferromagnetic and molecular. Molecular QCA is particularly attractive because of its projected density of 1×10^{12} devices/cm² and switching speeds in the THz range [2], [5].

Since QCA designs are limited by the availability of only two basic building blocks, researchers have tried to design, with limited success, additional gates in the QCA technology. For example, a five input AOI (AND-OR-INVERT) QCA gate giving $MAJ_3(x_0, x_1, MAJ_3(x_2, \overline{x_3}, \overline{x_4}))$ has been reported [6]. Unfortunately this gate uses an irregular placement of the cells which makes it unsuitable for larger architectures.

Prior designs of five-input majority gates also are not appealing [7]–[9]. For example, [9] provides a 3-Dimensional 5-input majority gate that requires a technology yet to be developed. It relies on applying inputs from all dimensions to ensure equal effect on the middle cell. A similar design in [7], shown in Fig. 2 (left) is planer but the output needs to be taken out from the middle cell. The output cell being surrounded by other cells is impossible to connect to without a multilayer design. The scheme shown in Fig. 2 (right) [8], avoids these pitfalls but the its inputs have to be applied from different angles, making it difficult to employ within larger architectures. Thus it retains the interface challenges (e.g., connections to inputs B and C). Clearly it is also more susceptible to faults. While a multi-layer solution is suggested for these connections, one should note that the multilayer QCA is not yet realizable.



Figure 2: Previous attempts to create a 5-input majority gate in QCA [7, 8].

3 A FIVE INPUT MAJORITY GATE

A five input majority gate, MAJ_5 , is a Boolean gate whose output is 1 only if 3 or more of its inputs are 1. The Boolean expression of MAJ_5 function is given by:

 $MAJ_{5}(A, B, C, D, E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE$

The proposed implementation of the MAJ_5 gate is shown in 3.

The MAJ_5 gate was simulated using the QCADesigner version 2.0.3 [10]. In all simulations given in this paper, we used the coherence vector computational engine and the following parameters: 10 $nm \times 10 nm$ cell size, 2.5 nm cell-to-cell distance, 2.5 nm dot size and 40 nm radius of influence. These are the same parameters employed by [11]–[13]. The simulation results are shown in Fig. 4. In these simulations that the polarization level of the output was quite satisfactory (±0.953).

4 APPLICATIONS

The five input majority gate MAJ_5 is extremely versatile and can be readily used to implement a variety of



Figure 3: A five input majority gate in the QCA technology.



Figure 4: Simulation output of the MAJ_5 gate shown in Fig. 3.

functions by tying some of inputs to constants and/or duplicating some inputs. The functions that can be directly implemented by MAJ_5 are given in Table 1. The table also gives the complexity of building the same functions using only MAJ_3 gates.

A serial adder can be designed with an inverter, a MAJ_3 gate and a MAJ_5 gate as in Fig. 5. It $addsa_{n-1}$, ..., a_1, a_0 and $b_{n-1}, \ldots, b_1, b_0$ to give s_n, \ldots, s_0, s_0 using

$$s_i = MAJ_5(a_i, b_i, c_{i-1}, \overline{c}_i, \overline{c}_i), \text{ where,}$$

$$c_i = MAJ_3(a_i, b_i, c_{i-1}).$$

Note the use of the feedback in Fig. 5 which enables one to employ c_{i-1} in the calculation of c_i and s_i . Since c_{-1} cannot be guaranteed to be 0, one may want to apply

(number of gates and the depth)gates required for the same function implementation. **Boolean** Function Inputs of MAJ_5 MAJ_3 imple. A_1 A_2 В C_1 C_2 gates depth \overline{XY} X 0 1 Y0 1 1 X + YX0 Y1 1 1 1

X

X

X

X

X

X

X

X

X

0

1

U

0

X

X

X

0

1

Y

Y

Y

Y

Y

Y

Y

Y

Y

Z

Z

Z

Z

Z

Z

Z

Z

Z

0

1

W

1

0

1

U

U

U

2

2

11

1

2

 $\mathbf{2}$

6

5

5

2

 $\mathbf{2}$

5

1

 $\mathbf{2}$

 $\mathbf{2}$

4

3

4

Table 1: Functions that can be implemented through a single MAJ_5 gate and comparison with MAJ_3 implementation



XYZ

X + Y + Z

X(Y+Z)

X + YZ

 $MAJ_3(X, Y, Z)$

 $MAJ_5(X, Y, Z, U, W)$

X(Y+Z+U)+YZU

X(YZ + YU + ZU) + YZU

X(Y+Z+U) + YZ + YU + ZU

Figure 5: A serial adder using a five input majority gate in the QCA technology.

0 at both A and B inputs of the circuit during the first clock period to flush the feedback path and ignore the sum bit during the corresponding output cycle. Figure 6 shows the simulation output of this serial adder.

Table 1 shows that a large number of complex Boolean functions can be realized through a single MAJ_5 gate. While these functions can also built from MAJ_3 gates, the hardware and the time complexity of these designs is generally fairly large as listed in Table 1.

5 A ROBUST FIVE INPUT MAJORITY GATE

Defects in QCA generally occur either during the *Chemical Synthesis* when the cells are manufactured, or during the *Deposition* when the cells are placed on the substrate. Studies suggest that the later of these defects has a greater probability of occurrence [14]. We therefore consider only the deposition defects. In par-



Figure 6: Simulation output for the adder shown in Fig. 5. The two input words B = 010111 and A = 011010 add to give the output word 110001.

ticular, we study here the effect of missing cells on the performance of the five input majority gate.

The MAJ_5 structure shown in Fig. 3 is quite susceptible to missing cells. Its robustness can, however be easily improved by enlarging the middle section as shown in Fig. 7. With an enlarged middle section, the contribution of a missing cell can be, at least partially, made up by its neighbors. This strategy has also been tried and proved successful in improving the robustness of a three input majority gate [11]. We find that for more than 40% of the defects (each defect is only one missing cell in the gate), the structure in Fig. 7 performs perfectly as intended. In particular if any one of the cells numbered 1, 3, 5, 6, 8, 14, 16, 18, 21, 23 or 25 is missing, the structure still performs as $MAJ_5(A_1, A_2, B, C_1, C_2)$.



Figure 7: A robust MAJ_5 gate with cells numbered.

6 CONCLUSION

This work reports design of a new planer five input majority gate (MAJ_5) for QCA applications. It can be easily interfaced with other gates in larger designs. A serial adder using this gate is developed and tested. A majority function MAJ_n is a special *n*-input threshold function with unit weights and a threshold value of $\lfloor n/2 \rfloor + 1$. As shown in Table 1 the MAJ_5 gate can be adapted to create many other complex threshold functions such as XYZ, X(Y + Z), X(Y + Z + U) + YZU, etc., each with varying weights and thresholds. General threshold functions have a much wider application domain [15]–[17] than just the majority functions. Extensions of the work reported here can thus lead to a plethora of new architectures in the QCA technology.

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