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Poly-Silicon TFT Backplanes on Flexible Metal Foils

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Why Metal Foils?

Advantages of Metal Foils vs. Plastics :

- Metal foils are readily compatible with polysilicon TFT technology due to superior thermal properties.
- Metal foils enable thermal oxidation to be used for gate dielectric for high performance & high reliability TFT circuits.
- Lower thermal expansion enables small design rules for high performance TFT circuits.
- Higher thermal conductivity enables dissipation of thermal loads.
- High conductivity of metal foils renders them useful as global power or ground terminal.
- Metal foils are excellent barriers to moisture thus ideal for OLEDs.
- Metal foils compatible with most wet chemical processes.

Maximum Process Temperature :

Plastics ~ 200 °C

Metal Foils ~ 1000 °C

Thermal Expansion Coefficients :

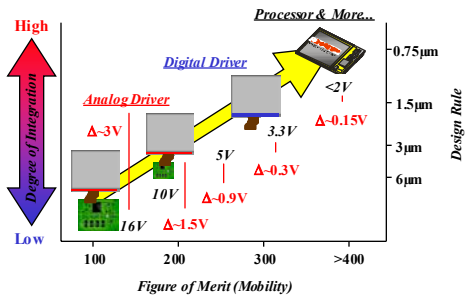
Dielectrics	Metals	Glass	PES	PET	PAR	PC	SS
5.5-7.5 ppm/°K	8.5-30 ppm/°K	5 ppm/°K	50 ppm/°K	70 ppm/°K	57 ppm/°K	20-50 ppm/°K	~20 ppm/°K

Irreversible Shrinkage After 1h of Pre-annealing :

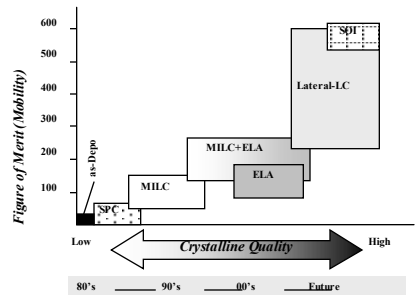
Glass [300°C/1h]	PES [190°C/1h]	PET [170°C/1h]	PAR [170°C/1h]	PC [130°C/1h]	SS [700°C/1h]
<10 ppm	10^3 ppm	10^3 ppm	10^2 ppm	10^2 ppm	40 ppm

Why Poly-Crystallized Silicon TFTs?

Requirements for Flexible Systems – High Performance TFTs (a-Si vs. poly-Si)



Evolution of Polysilicon Techniques -



SPC (Solid-Phase Crystallization) requires medium to high process temperatures. By heating amorphous silicon to temperatures above ~1/2 of its melting temperature atoms rearrange and form crystalline grains. Size of grains depend upon deposition and annealing conditions. By adding a catalyst (nickel) crystallization temperature can be reduced and material microstructure can improve.

Advantage: low cost. Problem: higher process temperature and inferior material quality compared to ELA

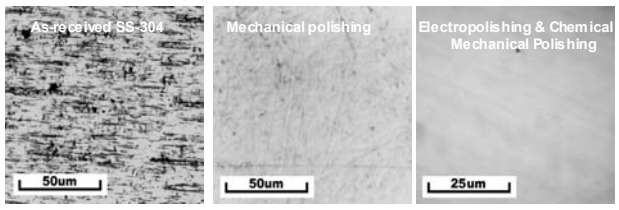
ELA (Excimer Laser Anneal) is a low temperature method. It relies in localized, rapid melting and solidification of Si. Hence, high quality material is produced w/o significantly heating the underlying substrate.

Advantage: high quality. Problem: high cost.

Metal foils are compatible with both ELA and SPC processes. Plastic substrates are only compatible with ELA.

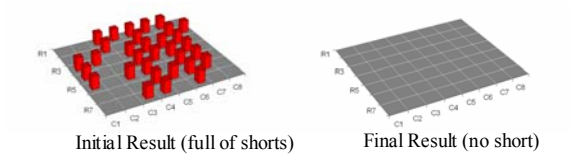
Substrates Preparation :

- Surface Polishing :



Surface finish with Ra less than 10 nm and TIR less than 100 nm can be achieved.

- Substrate Insulating Layers :



Initial Result (full of shorts) Final Result (no short)

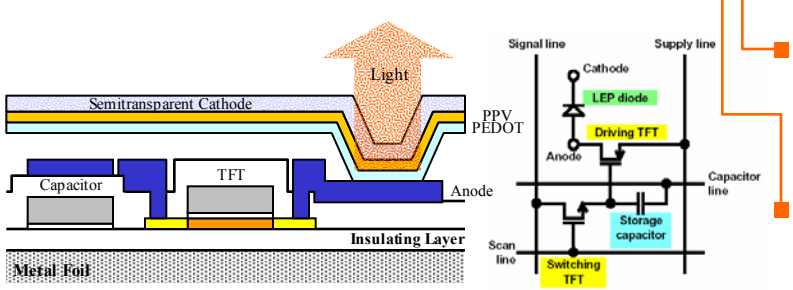
Testing Approach : Coat metal foil and then anneal at 900 °C. Evaporate aluminum through shadow mask that defines test pads of 1 cm2. Identify shorts between the 1 cm2 aluminum pads and metal foil substrate. 56 total sites were tested for each substrate (5 inch).

- Inter-Metal Insulating Layers :

Initial Result (full of shorts) Final Result (acceptable)

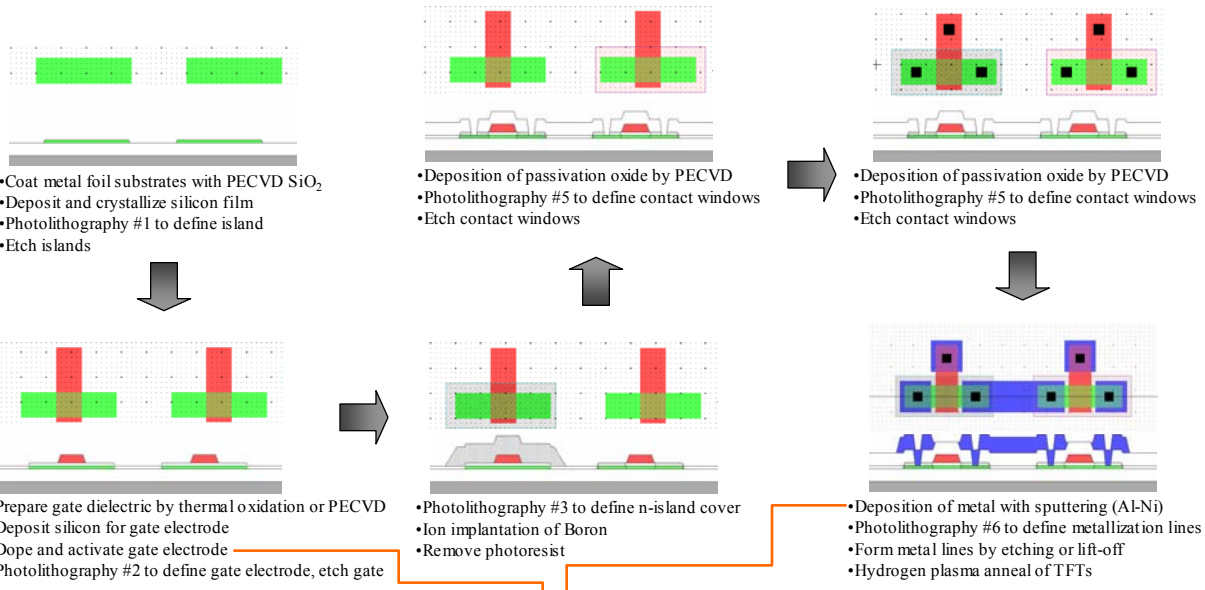
Each red lines indicates a group of 20 gate lines and each blue line indicates a group of 20 data lines that are shorted to power lines. After applying inter-metal dielectric layers, shorts were significantly reduced (from the left picture to the right).

Pixel Architecture :



- Each pixel is driven by two PMOS thin-film transistor. One transistor works as a switch, and the other one control the current passing through the light-emitting diode.
- Top-gate poly-silicon transistors are adopted, as well as the top-emitting polymeric light-emitting diodes.
- Prior to the fabrication of transistors, the substrate was well-polished and coated by an insulating layer.

Process Flow of CMOS TFT :



- Coat metal foil substrates with PECVD SiO_2
- Deposit and crystallize silicon film
- Photolithography #1 to define island
- Etch islands
- Prepare gate dielectric by thermal oxidation or PECVD
- Deposit silicon for gate electrode
- Dope and activate gate electrode
- Photolithography #2 to define gate electrode, etch gate
- Photolithography #3 to define n-island cover
- Ion implantation of Boron
- Remove photoresist
- Deposition of passivation oxide by PECVD
- Photolithography #5 to define contact windows
- Etch contact windows
- Deposition of passivation oxide by PECVD
- Photolithography #5 to define contact windows
- Etch contact windows
- Deposition of metal with sputtering (Al-Ni)
- Photolithography #6 to define metallization lines
- Form metal lines by etching or lift-off
- Hydrogen plasma anneal of TFTs

Processing Capabilities and Equipments :

PECVD: Gate dielectric and amorphous silicon deposition, and hydrogenation.

Perkin-Elmer Aligner: Capable of processing 6" silicon wafers and metal foils.

Technics Plasma Dry Etcher: Oxygen and CF_4 are available in this system. 1 um gate is achievable.

LPCVD: Thermal oxidation.

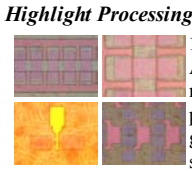
RF Magnetron Sputter with Thermal Evaporator: Three different targets can be placed in the system, and a thermal evaporator is also included.

Furnace: Post-doping activation, silicon crystallization, and annealing.

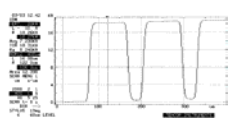
Tegal 920E RIE Dry Etcher: Reactive Ion Etcher is under installation.

E-beam Evaporator: A series of materials can be evaporated in this system, for instance, gold, titanium, platinum, aluminum, nickel, and silver. (Dept. of ECE at Lehigh U., Microelectronics Research Lab, Prof. Marvin White.)

Highlight Processing Capabilities :



1 micron poly-silicon gate on metal foils: After improving the surface finishing on the metal foils and optimizing the photolithography process as well as the dry etching process, a 1um gate can be obtained repeatedly not only on silicon wafers, but also on metal foils.



1.8um thick aluminum by lift-off process: A very thick aluminum layer can be implemented by this promising lift-off process and has the sheet resistance of 0.045 ohm/□.