

Low-loss quasi-planar ridge waveguides measured using ring resonators formed on thin silicon-on-insulator

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Motivation:

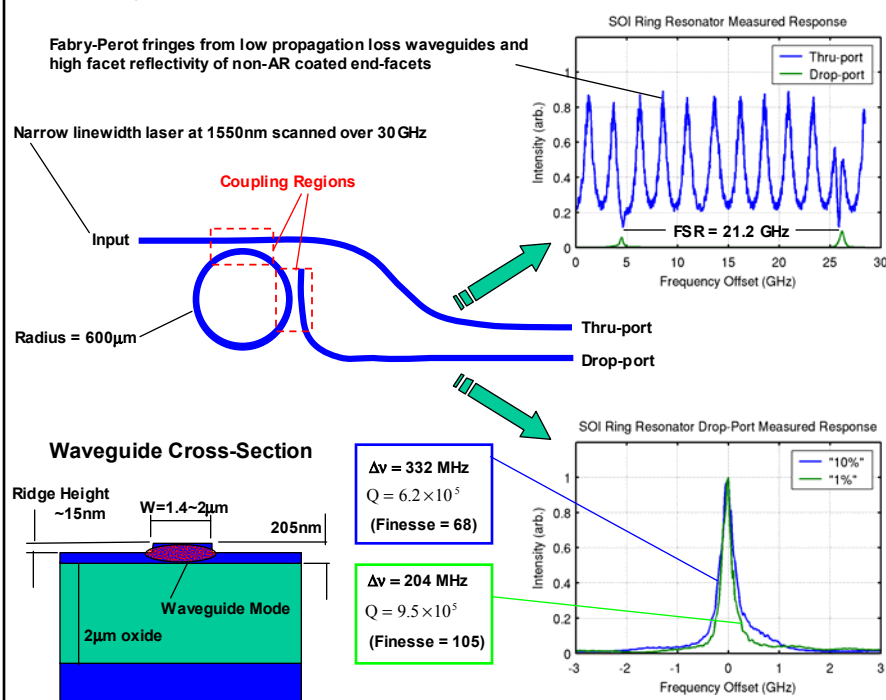
- Silicon-on-insulator (SOI) geometry very promising for guided-wave optical integration, leveraging mature Si process technology.
- High index contrast of SOI enables small waveguide geometries and low bending losses for high-density integration.
- Potential for full process compatibility with conventional CMOS silicon electronics for complex OEIC's.
- Strong desire for on-chip electrically driven optical gain to enable amplification and emitters (such as Er-based LEDs and lasers).

Challenge:

- Very challenging to minimize scattering losses from surface roughness due to high index contrast, $\alpha \sim (\Delta n)^2$

Ring Resonator Measurements

- For weak coupling of waveguides to ring, measuring the FWHM of the drop-port response at resonance enables the round-trip waveguide loss to be determined



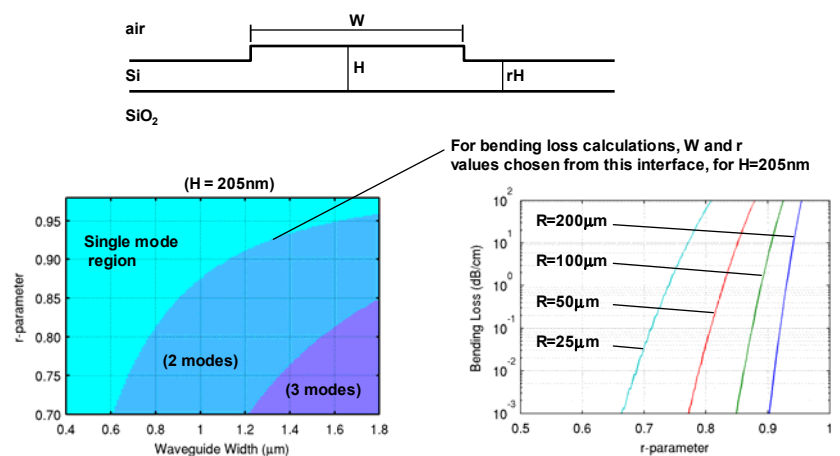
Measured waveguide propagation loss of < 0.7 dB/cm is among lowest reported for small modal-area SOI waveguides!

Future Work:

- Further investigate the loss mechanisms presently affecting SOI waveguides.
- Integrate Er-doped films into our quasi-planar ridge waveguide geometry and measure its optical characteristics.
- Study Raman effect in the small modal-area waveguides and ring resonators to produce a monolithic Raman laser.
- Fabricate active devices such as modulators compatible with quasi-planar ridge waveguide fabrication techniques.

Quasi-planar Ridge Waveguides

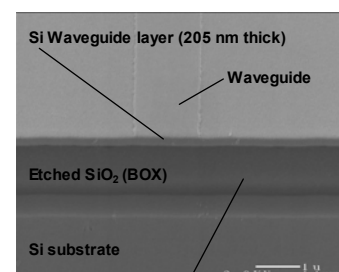
- Compatible with planar geometries desirable for proposed direct electrical injection of Er-doped thin films, for example.
- Scalable to achieve desired bending performance.



SOI Optical Waveguide Fabrication

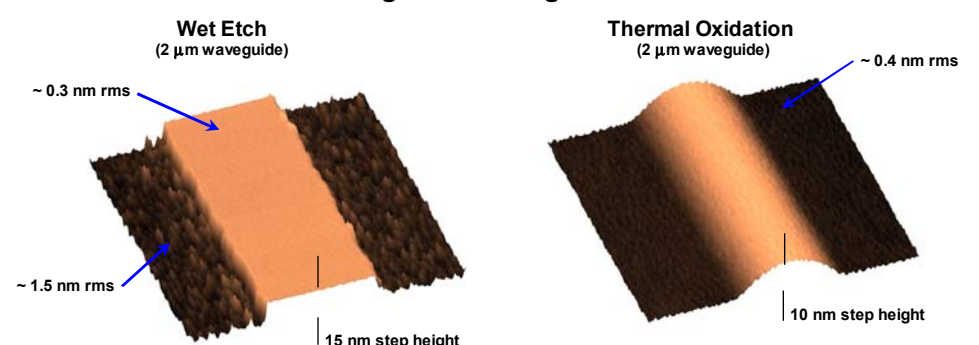
- Ridge waveguides formed using CMOS compatible processing
- Wet-etching of silicon used in an effort to minimize process induced surface roughness (such as from traditional RIE processing)

SEM image of waveguide end facet.



Waveguide facet was polished with PECVD SiO₂ over-cladding, then etched away (which also etched underlying BOX as well)

AFM images of waveguides



- Wet etching increases surface roughness of Si
- Thermal oxidation results in minimal surface roughness increase
- Thermal oxidation also reduces line-edge-roughness from photolithography