

## HgCdTe on Si Through Strain-Relieving Nanometer-Thin Buffer Layers

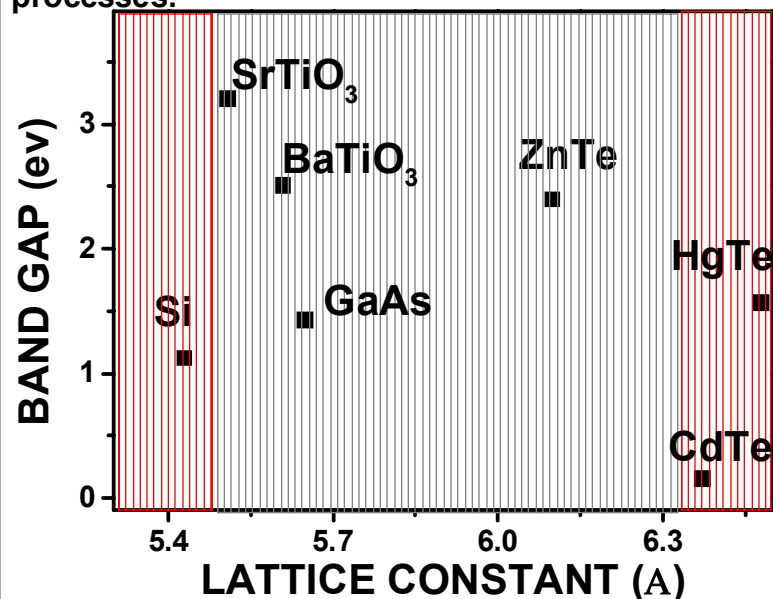
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### Purpose

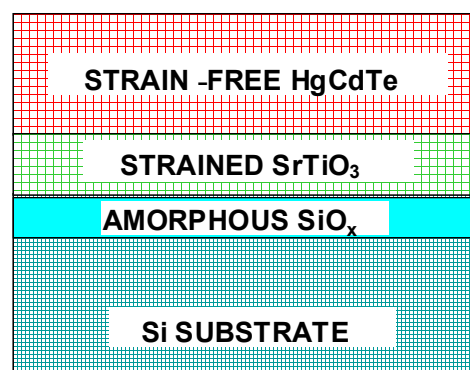
Monolithic integration of Si read-out circuits with HgCdTe infrared detectors. Take advantage of large diameter, inexpensive Si substrates. Reduce the cost and improve the reliability of infrared detectors such as focal plane arrays.

### Challenge

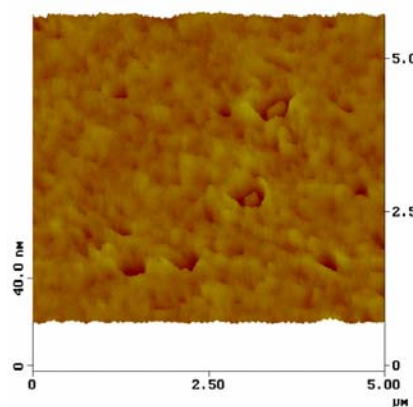
The 19% lattice mismatch between HgCdTe and Si leads to nucleation of dislocations, high dark currents, and reliability concerns. Currently, thick CdTe buffer layers are deposited on Si substrates. This process is expensive and incompatible with main-stream Si integrated circuit processes.



### Approach

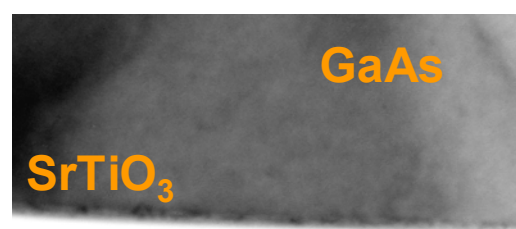


The unconventional approach employs a strain-relieving silicon-oxide nanometer-thick layer as has been demonstrated by Motorola for GaAs on Si, (Droopad et al. *J. Cryst. Growth*, 2002).

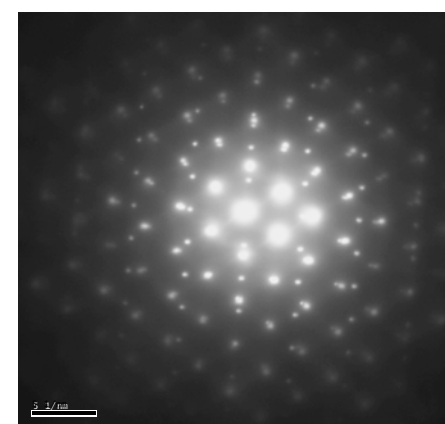


AFM\* image of a GaAs/SrTiO<sub>3</sub>/Si substrate. The top surface is very homogeneous, with small elevated features less than 15 nm tall.

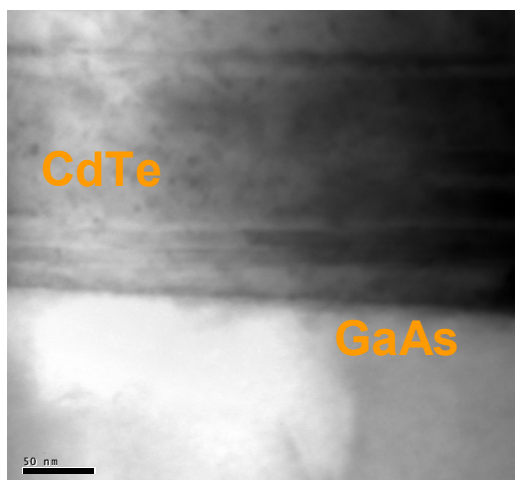
### Initial Growth Results



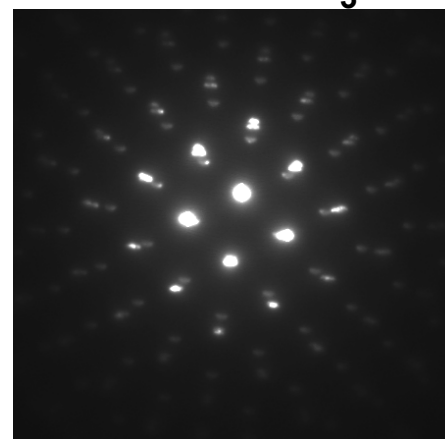
For the first time, CdTe has been grown on a GaAs/SrTiO<sub>3</sub>/Si compound substrate. Preliminary results indicate defect density in CdTe/GaAs/Si is comparable to that in CdTe/GaAs. Transmission electron microscopy shows sharp interfaces and dislocation loops instead of threading dislocations in CdTe/GaAs/SrTiO<sub>3</sub>/Si



GaAs/SrTiO<sub>3</sub>/Si



GaAs and CdTe have been nucleated epitaxially and are cubic single crystal, as seen in the diffraction patterns.



CdTe/GaAs

The good crystallinity of both SrTiO<sub>3</sub> and CdTe motivated the growth of BaTiO<sub>3</sub>, with a larger lattice parameter. The crystallinity of the system CdTe/BaTiO<sub>3</sub>/Si is currently under investigation.