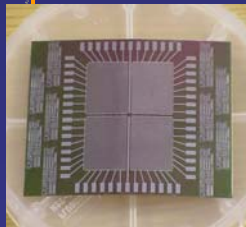


## Flexible Active Matrix Arrays and Electronics

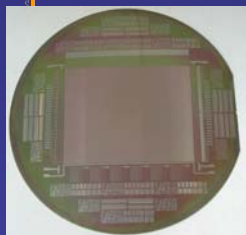
Matias Troccoli, Ta-Ko Chuang, Abbas Jamshidi, Grant Reed, Prof. M. Hatalis

### Evolution of our Poly-Silicon TFT Backplane Technology



#### 4 inch Steel Wafers:

- General Purpose Electronics
- 4 Arrays (60x80 pixels – 250um Pitch)
- Diagonal size: ~1 in
- Test Display driver circuits



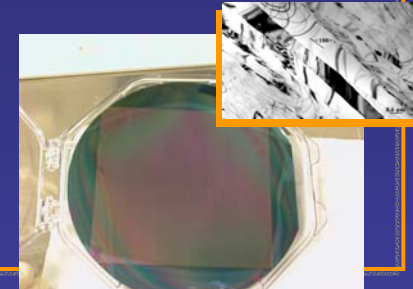
#### 5 inch Steel Wafers

- General Purpose Electronics
- 1 Array (640x480 pixels – 110um Pitch)
- Diagonal size: ~ 3 1/4 in
- Display row driver circuits integrated



#### 6 inch Laser Annealed Steel Wafers

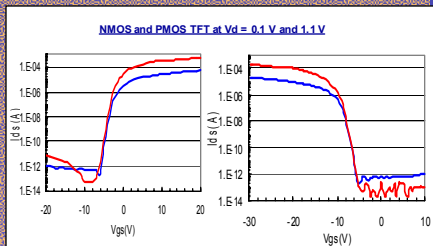
- Will include:
- 1 Array (640x480 pixels – 110um Pitch)
- Diagonal size: ~ 3 1/4 in
- Display row driver circuits integrated
- General Purpose Electronics



### High Performance Poly-silicon TFT

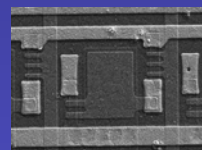


Low Temperature (300-600 °C) process (ELA + PECVD SiO<sub>2</sub> gate dielectric)  
High Temperature (800-1000 °C) process (SPC + thermal SiO<sub>2</sub> gate dielectric)

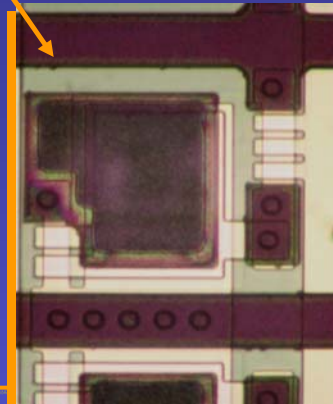


Gate Oxide	Device (W/L=20/4)	Mobility (cm <sup>2</sup> /Vs)	Vt (V)	SS (V/dec)	Ioff (A)
PECVD	NMOS	267	+1.4	1.4	1 pA
	PMOS	87	-9.8	2.4	0.1 pA
Thermal	NMOS	210	+2.3	2.6	1 pA
	PMOS	130	-3	3.4	1 pA

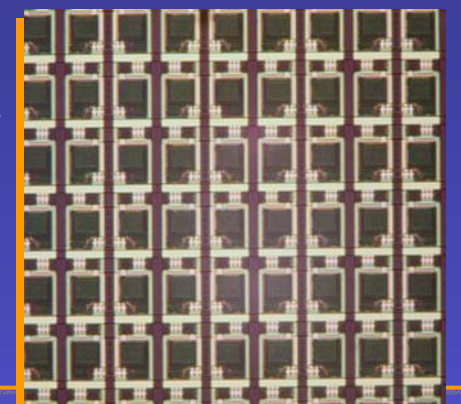
Optical Microscopy of finished active Pixel ready for deposition of Organic Materials.



SEM Shot of Active Pixel backplane on Stainless Steel foils fabricated at the Sherman Fairchild Labs at Lehigh University.

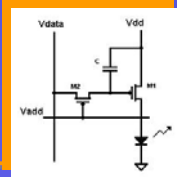


Active Matrix Array

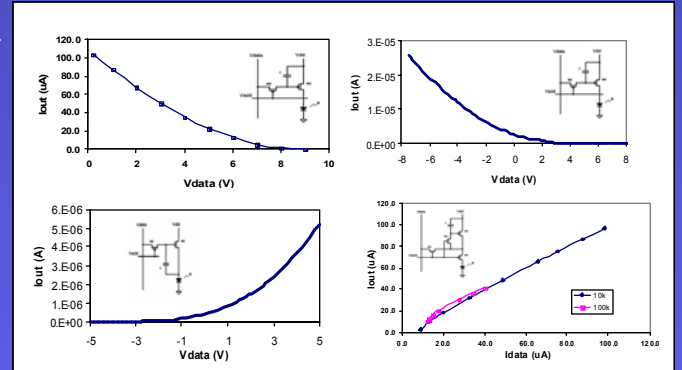


### Pixel Architecture: Two-TFT Pixel

- Advantages:
  - Simple proven benchmark design
  - Easy to control
- Disadvantages:
  - Display non-uniformity due to device parameter variations
- Shown output characteristics are for the following pixel implementations:



- 2 TFT 250 um Pitch - PMOS Architecture
- 2 TFT 125 um Pitch - CMOS Architecture
- 2 TFT 110 um Pitch - PMOS Architecture
- 4 TFT 250 um Pitch - CMOS Architecture



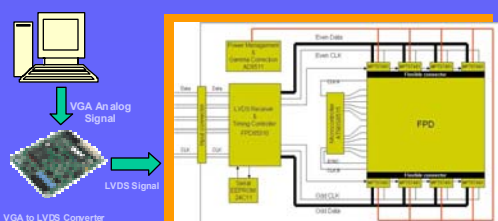
- When testing displays it is necessary to have great flexibility of control signals as well as ease of programmability of the interface software. With this in mind, two National Instruments PCI-6723 analog output cards are used to generate clock and data signals for the displays. The Lab-View programming environment was used to create virtual controls for the interface cards.  
- These cards can provide positive and negative output voltages of up to 10 Volts at refresh rates of up to 800 Ks/s (this high refresh rate allows us to drive the displays with frame rates of up to 50Hz).



Display Testing: Portable Block Driving Fixture



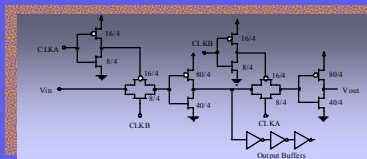
### LVDS based Custom Driver Board for full PC Interface



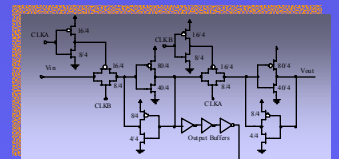
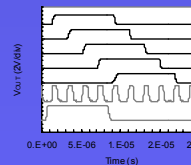
### Integrated TFT Display Drivers

#### Shift Registers

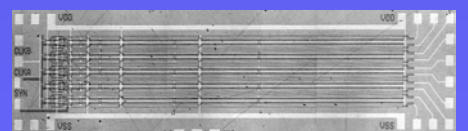
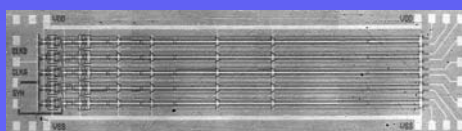
- Static and Dynamic Implementations of Shift registers have been implemented running at frequencies over 1 MHz.
- This makes them suitable for both row and column display driving.



Dynamic Shift Register Circuit and Picture with current buffers

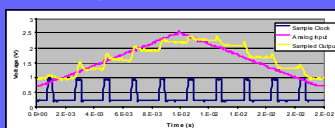


Static Shift Register Circuit and Picture with current buffers



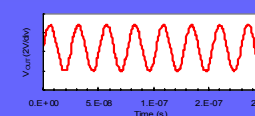
#### Sample and Hold

- CMOS Pass gate
- Integrated clock inverter for pass gate
- Analog buffer with long double gate differential pair for lower Kink Effects and higher linearity
- Large capacitor for retention of data for high resolution displays
- Just 125 um pitch



#### Ring Oscillator

- Ring Oscillator: 19 CMOS inverter stages, buffered output, 15V supply operation.
- Free-running frequency: 38MHz; translates in 3 ns prop. delay per inverter.



#### Digital to Analog Converter

- Implemented with resistor ladder for low transistor count
- Compatible with Voltage follower or Op-Amp implementations

